Course No.	Course Name	L-T-P-Credits	Year of Introduction
CS203	Switching Theory and Logic Design	3-1-0-4	2016

Pre-requisite: Nil

Course Objectives

1. To impart an understanding of the basic concepts of Boolean algebra and digital systems.
2. To impart familiarity with the design and implementation of different types of practically used sequential circuits.
3. To provide an introduction to use Hardware Description Language

Syllabus

Introduction to Number Systems, Boolean Algebra, Canonical Forms, Logic Gates, Digital Circuit Design, Combination Logic Circuit Design, Sequential Circuit Design, Registers, Counter, Memory modules, Programmable Logical Arrays, Hardware Description Language for Circuit Design, Arithmetic algorithms

Expected Outcome:

Students will be able to:-

1. apply the basic concepts of Boolean algebra for the simplification and implementation of logic functions using suitable gates namely NAND, NOR etc.
2. design simple Combinational Circuits such as Adders, Subtractors, Code Convertors, Decoders, Multiplexers, Magnitude Comparators etc.
3. design Sequential Circuits such as different types of Counters, Shift Registers, Serial Adders, Sequence Generators.
4. use Hardware Description Language for describing simple logic circuits.
5. apply algorithms for addition/subtraction operations on Binary, BCD and Floating Point Numbers.

Text Books:

1. Mano M. M., *Digital Logic & Computer Design*, 4/e, Pearson Education, 2013. [Chapters: 1, 2, 3, 4, 5, 6, 7].
2. Floyd T. L., *Digital Fundamentals*, 10/e, Pearson Education, 2009. [Chapters: 5, 6].
3. M. Morris Mano, *Computer System Architecture*, 3/e, Pearson Education, 2007. [Chapter 10.1, 10.2, 10.5, 10.6, 10.7].
4. Harris D. M. and, S. L. Harris, Digital *Design and Computer Architecture*, 2/e, Morgan Kaufmann Publishers, 2013 [Chapter 4.1, 4.2]

References:

1. Tokheim R. L., *Digital Electronics Principles and Applications*, 7/e, Tata McGraw Hill, 2007.
2. Mano M. M. and M. D Ciletti, *Digital Design*, 4/e, Pearson Education, 2008.
3. Rajaraman V. and T. Radhakrishnan, *An Introduction to Digital Computer Design*, 5/e, Prentice Hall India Private Limited, 2012.
4. Leach D, Malvino A P, Saha G, *Digital Principles and Applications, 8/e, McGraw Hill Education, 2015.*

COURSE PLAN

Module	Contents	Contact Hours (52)	Sem. Exam Marks;%

I	Number systems – Decimal, Binary, Octal and Hexadecimal – conversion from one system to another – representation of negative numbers – representation of BCD numbers – character representation – character coding schemes – ASCII – EBCDIC etc. Addition, subtraction, multiplication and division of binary numbers (no algorithms). Addition and subtraction of BCD, Octal and Hexadecimal numbers. Representation of floating point numbers – precision – addition, subtraction, multiplication and division of floating point numbers	**10**	**15%**
II	Introduction — Postulates of Boolean algebra – Canonical and Standard Forms — logic functions and gates methods of minimization of logic functions — Karnaugh map method and QuinMcClusky method Product-of-Sums Simplification — Don't-Care Conditions.	**09**	**15%**
III	Combinational Logic: combinational Circuits and design Procedure — binary adder and subtractor — multi—level NAND and NOR circuits — Exclusive-OR and Equivalence Functions. Implementation of combination logic: parallel adder, carry look ahead adder, BCD adder, code converter, magnitude comparator, decoder, multiplexer, de-multiplexer, parity generator.	**10**	**15%**
IV	Sequential logic circuits: latches and flip-flops – edge-triggering and level-triggering — RS, JK, D and T flip-flops — race condition — master-slave flip-flop. Clocked sequential circuits: state diagram — state reduction and assignment — design with state equations	**08**	**15%**
V	Registers: registers with parallel load - shift registers universal shift registers – application: serial adder. Counters: asynchronous counters — binary and BCD ripple counters — timing sequences — synchronous counters — up-down counter, BCD counter, Johnson counter — timing sequences and state diagrams.	**08**	**20%**

VI	Memory and Programmable Logic: Random-Access Memory (RAM)—Memory Decoding—Error Detection and Correction — Read only Memory (ROM), Programmable Logic Array (PLA). *HDL: fundamentals, combinational logic, adder, multiplexer.* Arithmetic algorithms: Algorithms for addition and subtraction of binary and BCD numbers, algorithms for floating point addition and subtraction.	**08**	**20%**

Question Paper Pattern:

1. There will be *five* parts in the question paper – A, B, C, D, E
2. Part A
   a. Total marks : 12
   b. *Four* questions each having *3* marks, uniformly covering module I and II; All *four* questions have to be answered.
3. Part B
   a. Total marks : 18
   b. *Three* questions each having *9* marks, uniformly covering module I and II; T*wo* questions have to be answered. Each question can have a maximum of three subparts
4. Part C
   a. Total marks : 12
   b. *Four* questions each having *3* marks, uniformly covering module III and IV; All *four* questions have to be answered.
5. Part D
   a. Total marks : 18
   b. *Three* questions each having *9* marks, uniformly covering module III and IV; T*wo* questions have to be answered. Each question can have a maximum of three subparts
6. Part E
   a. Total Marks: 40
   b. *Six* questions each carrying 10 marks, uniformly covering modules V and VI; *four* questions have to be answered.
   c. A question can have a maximum of three sub-parts.
7. There should be at least 60% analytical/design/numerical questions.