Multicore Processors

Vipin Vasu

Outline

Need For MultiCore

- Moores law gives us free increase in performance over time.
- The increase in transistors results in increase in switching and leakage power.
- Increased performance from Moores Law also requires CPUs to run at higher clock speed resulting in increased power usage.

Multicore designs were brought about to manage power consumption without any loss in performance.

Technical Motivation

- The power dissipation of a CPU is directly proportional to of its clock frequency and quadratic with supply voltage.
- However a decrease in frequency also results in a proportional decrease in supply voltage.
- Thus, reducing frequency can result in a dramatic decrease in power dissipation.
- This allows for the possibility of placing another core on the die while keeping power consumption same as before.
- The performance of the multicore chip is given as: Pm = (1 + Ep)pm where Ep is the reduction in performance due to reduced clock frequency, p is the power of the single fast core m is the number of cores For multicore to be effective we can clearly see that Ep should be larger than (1/m) - 1

Implementation

- The cores on a single die can have separate caches or share certain levels. A group of cores that share a certain level of cache is called a cache group
- The advantage of shared caches is that it allows for faster communication between cores.
- However it can also result in cache bandwidth bottlenecks
- Recent designs incorporate an integrated memory controller to which memory modules can be attached directly resulting in faster memory access

Conclusion

- First of all, in a multicore environment we must be able to efficiently use all available resources through parallel programming
- A challenge faced by multicore design is the reduced memory bandwidth and cache size. This can affect the performance of certain algorithms. Hence, algorithms to manage traffic and contention for shared resources such as memory, memory bandwidth are important

The End